A 12 WATT 20 GHz FET POWER AMPLIFIER

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ABSTRACT

A state of the art 20 GHz GaAs FET power amplifier with a maximum output of 12 watts and 15.5% power added efficiency has been developed. The amplifier utilizes a novel 2.0 watt power FET design that incorporates partial input impedance matching circuitry on the FET die to improve bandwidth performance and repeatability. Single ended and balanced power modules were combined with low loss waveguide hybrids in a planar amplifier designed to be compatible with integration into satellite systems.

INTRODUCTION

The application of high power, high efficiency GaAs FET solid state power amplifiers (SSPAs) for satellite downlinks has been proceeding slowly, due to inadequate device performance. To provide small, reliable and efficient 20 GHz wideband solid state transmitters, device performance needed to be improved [1][2]. Recent advancements in 20 GHz power FET technology have led to the development of a GaAs FET device which produced 2 watts (+33 dBm) of output power with 30% power added efficiency and 5 dB associated gain. These devices utilize on-chip partial input matching, which allows for multi-GHz bandwidth performance. This performance is believed to be the highest output power and efficiency reported for a 20 GHz GaAs FET.

This paper describes the results achieved by combining 8 power devices in multi-watt modules using low loss waveguide combiners to obtain 12 watts of output power with 15.5% power added efficiency. These state of the art results were produced using a planar amplifier configuration which is readily adaptable to most spacecraft. Each module was fabricated using space-flight approved materials and processes.

DEVICE DESIGN

The baseline FET used to build the 12 watt SSPA was a 2 watt device designed and fabricated at Avantek, Inc. This design is referred to as an OM-FET, an abbreviation for on-chip matched FET.

The total gate periphery of the OM-FET is 4.8 mm. To realize a 4.8 mm device in a span considerably less than one wavelength at 20 GHz, it is necessary to optimize the gate finger width, G-G pitch, and device size. This design was composed of eight basic cells, optimized for K-band applications. As shown in Figure 1, each cell consists of ten gate fingers, and each finger is 0.5 µm in length and 60µm in width. A S-D spacing of 4.5 µm and a G-G pitch of 18.5 µm were designed in consideration of gain performance and thermal resistance. The same structure has been used in an Avantek 7.2 mm device, which demonstrated superior performance at Ku band [3].

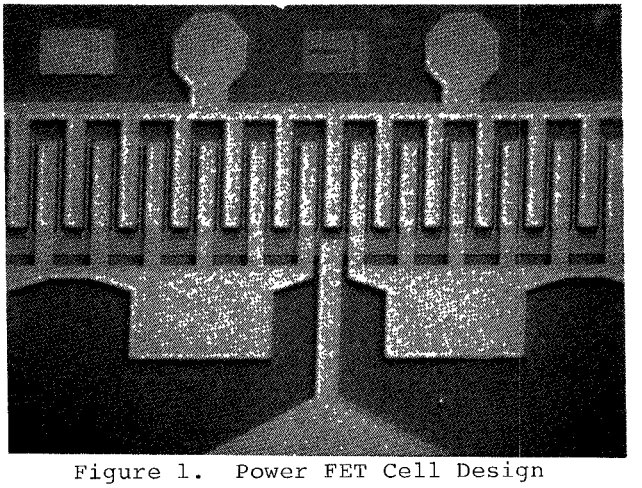

Figure 1. Power FET Cell Design

To achieve broadband performance, a partial impedance matching network was fabricated on the OM-FET chip. As shown in Figure 2, a short high impedance line is used to resonate the device gate capacitance, while low impedance transmission lines are used to raise the device input impedance from 1 ohm to approximately 8 ohms. The GaAs chip thickness of 1.5 mils and the chip size of 69 mils x 55 mils were designed to realize the on-chip low impedance transmission lines. The

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remaining input and output matching circuits were fabricated on external alumina substrates.

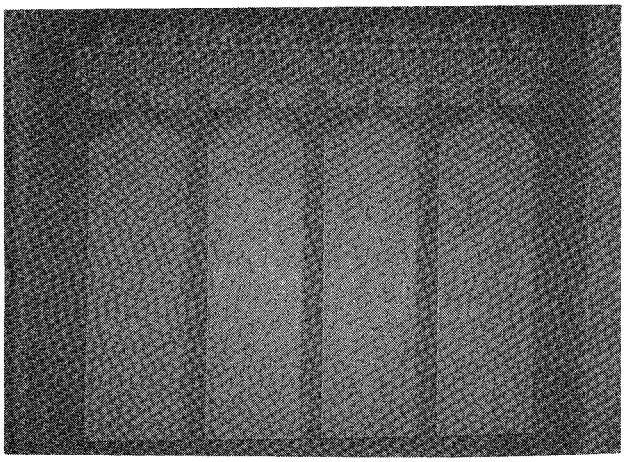

Figure 2. OM-FET Matching Structure

DEVICE FABRICATION

Material selection and device fabrication are key to the power FET performance. High quality GaAs epitaxial material grown by both VPE and MBE methods were used for device fabrication. The VPE material has a simple structure of an n active layer on top of a high purity layer grown on the Cr doped substrates. The MBE material has an n + layer for contact purpose and an n active layer following a p type buffer layer grown on the LEC substrates.

The FET front-side fabrication has been described in detail elsewhere [3]. A backside via hole process was used to reduce the source grounding inductance, which greatly effects the device performance at high frequencies. The DC qualified wafers were thinned to 1.5 mils, and well defined via-holes were etched in a reactive ion etcher. Thick gold was then plated for source grounding, heat sinking, and chip supporting purposes.

MODULE DESIGN

An equivalent circuit model and load-line analysis were used to analyze potential FET matching circuitry. Based on preliminary analysis, it was determined that it would be extremely difficult for a 2 watt, 20 GHz power FET to achieve a repeatable broadband input match using standard external matching techniques. Analysis showed that by eliminating input bond wire variation and providing partial input impedance transformation, broadband performance should be achievable with greatly improved tuning repeatability. The on-chip matching network that was derived consisted of a short inductive section to resonate the gate capacitance and quarterwave transformers to raise the input impedance to approximately 8 ohms. The remaining input matching and drain matching were achieved using external matching circuits on alumina substrates.

Single ended and balanced modules were designed to provide nominal 2 watt and 3.5 watt amplifier building blocks. A 15 mil thick alumina substrate was chosen as the baseline thickness for this 20 GHz power application. To eliminate or reduce circuit parasitics, several components were fabricated on the matching circuit substrates. Thin film tantulum nitride resistors were used to provide oscillation suppression networks and DC bias networks. Interdigitated blocking capacitors and Lange hybrids were fabricated on the balanced module substrates. The Lange hybrids were fabricated with dielectric supported crossovers to eliminate the need for wirebonds. Measured Lange hybrid loss was less than .15 dB. Parallel plate capacitors were used to provide RF bypass capacitors. The single ended and balanced modules are shown in Figure 3.

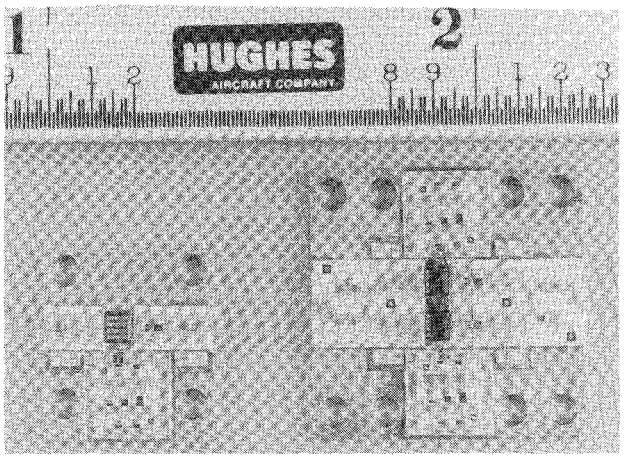

Figure 3. 2.0 and 3.5 Watt Modules

Both module designs used gold plated OFHC copper carriers to reduce thermal resistance. The FETs, substrates, and components were attached with gold eutectic solders for high reliability. All interconnects were done by thermocompression bonding. A key mechanical feature of these designs was the attachable walls, which provide a channel below waveguide cutoff. This feature reduces radiation effects and thus improves tuning consistency.

Both designs were subjected to space-flight environmental qualification testing to confirm mechanical integrity. These tests included vibration, thermal shock,

and thermal cycling.

MODULE PERFORMANCE

The modules were evaluated using test fixture that incorporated Wiltron K connectors. All module data was corrected for connector losses. Initially, all wafers were evaluated in the single ended module design to characterize wafer performance. Each module was tuned for broadband power gain with a goal of 1 dB bandwidth greater than 2 GHz.

The best measured data demonstrated 2 watts output power with 5 dB associated gain and 30% power added efficiency. These results are believed to be the highest efficiency data for a 2 watt, 20 GHz power FET. At the time the amplifier modules were built, wafers with more typical performance were used. Figure 4 is a summary of best wafer performance and typical module performance used in the 12-watt amplifier.

AMPLIFIER DESIGN

The 12-watt amplfier was designed using the building blocks of the single ended 2 watt module and the balanced 3.5 watt module. In order to efficiently achieve the desired 12 watts of output power, it was necessary to combine eight power FETs using both low loss microstrip and waveguide power combiners.

The first level of power combining, at the 3.5 watt module level, was achieved in microstrip by fabricating Lange hybrids. The loss of these Lange hybrids was approximately .15 dB. The final level of power combining was performed in waveguide, using short slot hybrids in a 4-way configuration. Waveguide was chosen for this level because of it's inherent low loss characteristics, which were measured to be approximately .10 dB for the 4-way combiner.

By utilizing a binary type power combiner (N = 2,4,8, etc.), the amplifier can be easily constructed in a planar configuration. The planar configuration allows for proper heat sinking of the amplifier housings, which reduces the amplifier's thermal resistance. This also allows for the amplifier to be easily integrated with existing satellite thermal control systems.

The amplifier housings are designed to be modular so that module designs can be minimized. Each housing is constructed of two single ended amplifier modules followed by a balanced amplifier power stage, as shown in Figure 5.

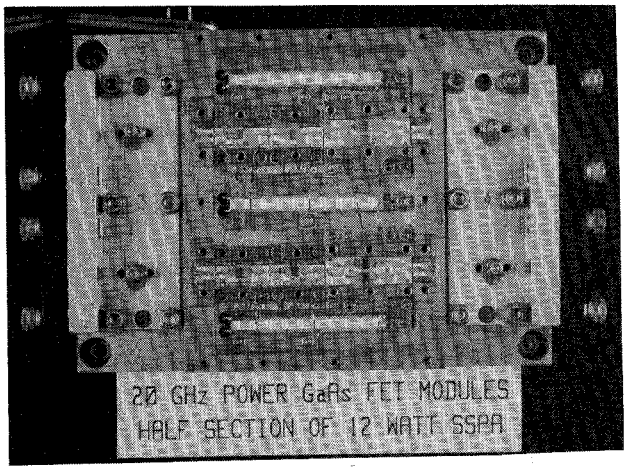

Figure 5. Power Amplifier Housing

The waveguide-to-microstrip transitions were constructed using a hermetic feedthru launched into the waveguide using a tapered ridge transformer. The loss of these transistions were measured to be less than .2 dB.

AMPLIFIER PERFORMANCE

State of the art performance has been achieved for a solid state power amplifier operating at 20 GHz. The saturated output power of the amplifier was 12 watts with

Module Type	POUT (Watts)	Gain (ASSOC) dB	EFF (P.A.) %	BW (1dB) GHz	Comments	Wafer Type
Single Ended	2.0	5.0	30	2.0	Best data	MBE (n+/n)
Single Ended	1.5	5.0	25	2.0	Typical Amp. Modules	MBE (n+/n)
Balanced	3.2	4.5	17	2.0	Typical Amp. Modules	VPE

Figure 4. Module Performance Summary

an associated power added efficiency of 15.5%, as shown in Figure 6. This amplifier exhibited a large signal instantaneous bandwidth of 1.7 GHz. The frequency response of ths amplifier is shown in Figure 7.

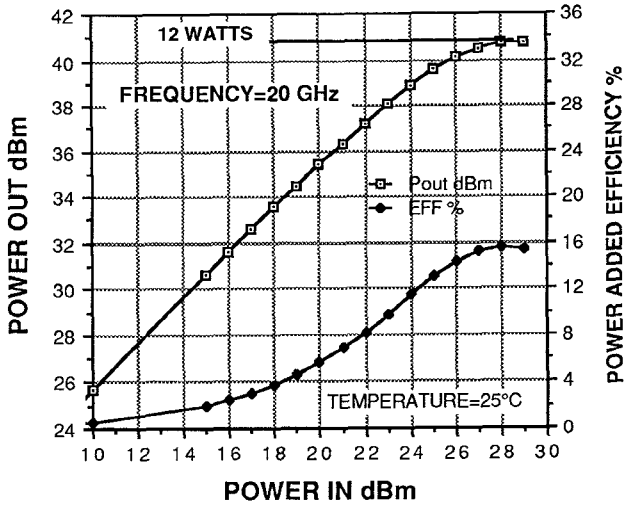

Figure 6. Power Compression Data

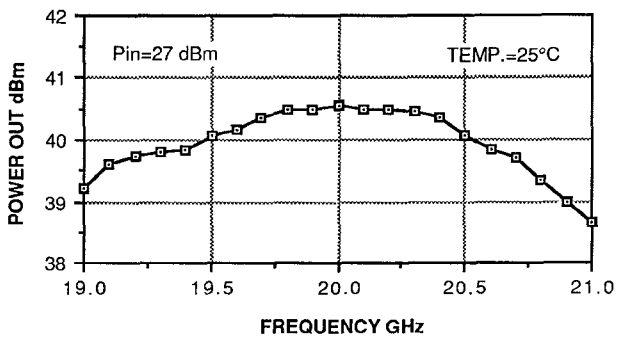

Figure 7. Amplifier Frequency Response

The amplifier was characterized over a temperature range of -30°C to +70°C. The performance variation over this temperature range was less than .2 dB/10°C. Although this is a very extreme temperature delta, the performance variation is considered very good and can be improved by using temperature compensation circuitry.

CONCLUSION

State of the art results have been demonstrated for 20 GHz power FETs and SSPAs. A unique FET design with partial input matching on the FET die has demonstrated 2 watts output power and 30% efficiency. In addition, a 12 watt SSPA with 15.5% efficiency and a 1 dB bandwidth of 1.7 GHz has been demonstrated. This SSPA was built using space-flight approved processes and a mechanical design that would allow easy integration into a satellite system. With recent advancements in FET processing and structures, it is projected that in the next few years devices will improve sufficiently to allow satellite designers to offer high efficiency multi-watt, 20 GHz SSPA downlinks.

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